

# CMOS PLL SYNTHESIZERS

Analysis and Design

Keliu Shu  
Edgar Sánchez-Sinencio

 Springer

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# **CMOS PLL Synthesizers: Analysis and Design**

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# Contents

<b>List of Acronyms and Symbols</b>	ix
<b>Preface</b>	xv
<b>1 Introduction</b>	1
1.1 MOTIVATION	1
1.2 SUMMARY OF BOOK	2
1.3 BOOK ORGANIZATION	4
REFERENCES	5
<b>2 Frequency Synthesizer for Wireless Applications</b>	7
2.1 DEFINITION AND CHARACTERISTICS	7
2.2 PHASE NOISE AND TIMING JITTER	8
2.2.1 Phase noise and spurious tone .....	8
2.2.2 Timing jitter .....	11
2.3 IMPLEMENTATION OF FREQUENCY SYNTHESIZER	14
2.3.1 Direct analog frequency synthesizer.....	14
2.3.2 Direct digital frequency synthesizer .....	15
2.3.3 PLL-based frequency synthesizer.....	16
2.3.4 DLL-based frequency synthesizer .....	20
2.3.5 Hybrid frequency synthesizer .....	21
2.3.6 Summary and comparison of synthesizers.....	21
2.4 FREQUENCY SYNTHESIZER FOR WIRELESS TRANSCEIVERS	22
2.5 OTHER APPLICATIONS OF PLL AND FREQUENCY SYNTHESIZER	24
REFERENCES	26

<b>3 PLL Frequency Synthesizer</b>	<b>31</b>
3.1 PLL FREQUENCY SYNTHESIZER BASICS	31
3.1.1 Basic building blocks of charge-pump PLL .....	31
3.1.2 Continuous-time linear phase analysis .....	34
3.1.3 Locking time .....	44
3.1.4 Tracking and acquisition .....	56
3.2 FAST-LOCKING TECHNIQUES	58
3.2.1 Bandwidth gear-shifting .....	58
3.2.2 VCO pre-tuning .....	60
3.3 DISCRETE-TIME ANALYSIS AND NONLINEAR MODELING	60
3.3.1 z-domain transfer function and stability analysis .....	60
3.3.2 Nonlinear dynamic behavior modeling .....	62
3.4 DESIGN EXAMPLE: 2.4GHZ INTEGER-N PLL FOR BLUETOOTH	62
REFERENCES	65
<b>4 <math>\Sigma\Delta</math> Fractional-N PLL Synthesizer</b>	<b>69</b>
4.1 $\Sigma\Delta$ FRACTIONAL-N FREQUENCY SYNTHESIZER	69
4.1.1 $\Sigma\Delta$ quantization noise to phase noise mapping .....	70
4.1.2 $\Sigma\Delta$ quantization noise to timing jitter mapping .....	73
4.2 A COMPARATIVE STUDY OF DIGITAL $\Sigma\Delta$ MODULATORS	73
4.2.1 Design considerations .....	73
4.2.2 Four types of digital $\Sigma\Delta$ modulators .....	74
4.2.3 Summary of comparative study .....	87
4.3 OTHER APPLICATIONS OF $\Sigma\Delta$ -PLL	90
4.3.1 Direct digital modulation .....	90
4.3.2 Frequency-to-digital conversion .....	91
4.4 MODELING AND SIMULATION OF $\Sigma\Delta$ -PLL	92
4.5 DESIGN EXAMPLE: 900MHz $\Sigma\Delta$ -PLL FOR GSM	95
REFERENCES	98
<b>5 Enhanced Phase Switching Prescaler</b>	<b>103</b>
5.1 PRESCALER ARCHITECTURE	103
5.1.1 Conventional prescaler .....	103
5.1.2 Phase switching prescaler .....	105
5.1.3 Injection-locked prescaler .....	107
5.1.4 Summary and comparison of prescalers .....	107
5.2 ENHANCED PHASE-SWITCHING PRESCALER	108
5.3 CIRCUIT DESIGN AND SIMULATION RESULTS	110
5.3.1 Eight 45°-spaced phases generation .....	110
5.3.2 8-to-1 multiplexer .....	111
5.3.3 Switching control circuit .....	112
5.3.4 Asynchronous frequency divider .....	113
5.4 DELAY BUDGET IN THE SWITCHING CONTROL LOOP	115

5.5 SPURS DUE TO NONIDEAL 45° PHASE SPACING	117
REFERENCES	123
<b>6 Loop Filter With Capacitance Multiplier</b>	<b>127</b>
6.1 LOOP FILTER ARCHITECTURE	127
6.1.1 Passive loop filter .....	127
6.1.2 Dual-path loop filter.....	128
6.1.3 Sample-reset loop filter.....	131
6.1.4 Other loop filter architectures.....	133
6.1.5 Summary and comparison of loop filters.....	137
6.2 LOOP FILTER AND CHARGE-PUMP NOISE MAPPING	138
6.3 LOOP FILTER WITH CAPACITANCE MULTIPLIER	141
6.3.1 Third-order passive loop filter .....	141
6.3.2 Capacitance multiplier.....	142
6.3.3 Simulation of loop filter with capacitance multiplier .....	145
6.3.4 Noise consideration .....	148
REFERENCES	149
<b>7 Other Building Blocks of PLL</b>	<b>151</b>
7.1 VCO	151
7.1.1 LC-VCO .....	151
7.1.2 Varactor .....	152
7.1.3 Inductor.....	155
7.1.4 VCO phase noise .....	156
7.1.5 Layout.....	161
7.2 PHASE-FREQUENCY DETECTOR	162
7.3 CHARGE-PUMP	164
7.3.1 Reference spur .....	164
7.3.2 Charge pump architectures .....	171
7.4 PROGRAMMABLE DIVIDER	173
7.5 DIGITAL $\Sigma\Delta$ MODULATOR	176
7.6 CHIP LAYOUT	176
REFERENCES	178
<b>8 Prototype Measurement Results</b>	<b>183</b>
8.1 PRESCALER MEASUREMENT	183
8.2 LOOP FILTER MEASUREMENT	186
8.3 PLL MEASUREMENT	188
REFERENCES	194
<b>9 Conclusions</b>	<b>195</b>
<b>Appendix</b>	<b>199</b>





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## List of Acronyms and Symbols

AAC	Automatic Amplitude Control
BPF	Band-Pass Filter
CCO	Current-Controlled Oscillator
CDR	Clock and Data Recovery
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge-Pump
DAC	Digital-to-Analog Converter
DAS	Direct Analog Synthesizer
DDS	Direct Digital Synthesizer
DFDD	Digital Frequency Difference Detector
DLL	Delay-Locked Loop
DPA	Digital Phase Accumulator
DUT	Device Under Test
FDC	Frequency-to-Digital Converter
FF	Flip-Flop
FHSS	Frequency-Hopping Spread Spectrum
FM	Frequency Modulation
FN	Fractional-N
FS	Frequency Synthesizer
GSM	Global System for Mobile communications
IC	Integrated Circuit
ILFD	Injection-Locked Frequency Divider
ISF	Impulse Sensitivity Factor
ISM	Industrial Scientific Medicine
LF	Loop Filter
LO	Local Oscillator
LTI	Linear Time-Invariant
LSB	Least-Significant-Bit

MASH	Multi-stage noise Shaping
NAND	Negative AND logic
NCO	Numerically Controlled Oscillator
NMOS	N-channel Metal Oxide Semiconductor
NOR	Negative OR logic
OPA	Operational Amplifier
OSR	Over Sampling Ratio
OTA	Operational Transconductance Amplifier
PD	Phase Detector
PFD	Phase-Frequency Detector
PGS	Patterned Ground Shield
PLL	Phase-Locked Loop
PMOS	P-channel Metal Oxide Semiconductor
PSD	Power Spectral Density
RF	Radio Frequency
<i>rms</i>	Root-Mean-Square
SC	Switched Capacitor
SCL	Source-Coupled Logic
SDM	Sigma-Delta Modulator
SNR	Signal-to-Noise Ratio
SSB	Single-Sideband
TSPC	True-Single-Phase-Clock
VCO	Voltage-Controlled Oscillator
XOR	Exclusive OR logic
$\omega$	angular frequency in <i>rad/s</i>
$\omega_{-3dB}$	PLL $-3dB$ loop bandwidth
$\omega_c$	PLL loop (unity-gain / crossover) bandwidth
$\omega_{c1}$	1 <sup>st</sup> corner frequency of capacitance multiplier impedance
$\omega_{c2}$	2 <sup>nd</sup> corner frequency of capacitance multiplier impedance
$\omega_{c3}$	3 <sup>rd</sup> corner frequency of capacitance multiplier impedance
$\omega_n$	natural frequency
$\omega_{p1}$	1 <sup>st</sup> pole-frequency of loop filter transimpedance
$\omega_{p2}$	2 <sup>nd</sup> pole-frequency of loop filter transimpedance
$\omega_{p3}$	3 <sup>rd</sup> pole-frequency of loop filter transimpedance
$\omega_{ref}$	PLL reference angular frequency (at PFD)
$\omega_z$	zero-frequency of loop filter
$\omega_{1/f}$	corner angular frequency of $1/f$ noise
$\Delta\omega_{1/f^3}$	corner angular frequency of oscillator $1/f^3$ phase noise

$\Delta\omega$	angular frequency offset from carrier
$\Delta\omega_H$	PLL hold range
$\Delta\omega_L$	PLL lock range
$\Delta\omega_P$	PLL pull-in range
$\Delta\omega_{PO}$	PLL pull-out range
$\phi$	phase
$\phi_m$	phase margin
$\Delta\phi$	amplitude of phase modulation
$\Delta\phi_{rms}$	PLL output <i>rms</i> phase noise
$\theta$	phase
$\theta_e$	phase error at PFD inputs
$\theta_{in}$	input phase (noise)
$\theta_{out}$	output phase (noise)
$\theta_{vco}$	VCO phase noise
$\varphi$	random phase variation
$\zeta$	damping factor
$\varepsilon$	normalized settling frequency error of PLL
$\mathcal{L}$	phase noise in <i>dBc/Hz</i>
$\sigma_c$	<i>rms</i> of cycle jitter
$\sigma_{cc}$	<i>rms</i> of cycle-to-cycle jitter
$\tau$	time
$\delta$	impulse function (Dirac delta function)
$\delta_T$	periodic impulse function with period <i>T</i>
$\Gamma$	ISF function
$B$	current ratio
$C_1$	1 <sup>st</sup> capacitance of passive loop filter
$C_2$	2 <sup>nd</sup> capacitance of passive loop filter
$C_3$	3 <sup>rd</sup> capacitance of passive loop filter
$C_{p1}$	1 <sup>st</sup> parasitic capacitance of capacitance multiplier
$C_{p2}$	2 <sup>nd</sup> parasitic capacitance of capacitance multiplier
$f$	frequency in <i>Hz</i>
$f_0$	carrier frequency
$f_c$	PLL loop (unity-gain / crossover) bandwidth
$f_{div}$	loop divider output frequency
$f_m$	modulation frequency

$f_{ref}$	PLL reference frequency (at PFD)
$f_{vco}$	VCO frequency
$f_{RF}$	RF frequency (of mixer)
$f_{LO}$	local oscillator frequency
$\Delta f$	offset frequency from the carrier
$\Delta f_{1/f^3}$	corner frequency of oscillator $1/f^3$ phase noise
$F$	active device noise factor
$g$	conductance, transconductance
$G$	conductance, transconductance
$h$	transfer function
$H$	transfer function
$H_{cl}$	PLL closed-loop input-to-output phase (noise) transfer function
$H_e$	PLL input phase (noise) to PFD phase error transfer function
$H_{ol}$	PLL open-loop input-to-output phase (noise) transfer function
$H_{Vc}$	PLL input phase to LF output voltage transfer function
$i$	current
$i_{cp}$	charge-pump current noise
$I$	current
	in-phase signal
$I_c$	control current of CCO
$I_{cp}$	charge-pump current
$I_{cpi}$	charge-pump current of integration path
$I_{cpp}$	charge-pump current of proportional path
$I_{dn}$	charge-pump current for discharging the load capacitor
$I_p$	output current of LF's proportional path
$I_{up}$	charge-pump current for charging the load capacitor
$I_z$	output current of LF's integration path
$j$	integer number
$k$	binary integer input of DPA or digital SDM Boltzmann constant
$K$	PLL loop gain
$K_{pd}$	PFD and charge-pump gain in $A/rad$
$K_{vco}$	VCO conversion gain in $rad/s/V$
$K_{cco}$	CCO conversion gain in $rad/s/A$

$L$	integer number (order of SDM) inductance
$m$	integer number
$M$	modulus of DPA or digital SDM
$n$	integer number
$n_Q$	output integer of digital SDM
$N$	number (nominal) frequency divide ratio of loop divider
$N_B$	integer part of fractional-N divide ratio
$P$	prescaler divide ratio power
$P_r$	PLL reference spur level in $dBc$
$q$	charge
$Q$	quadrature signal quality factor quantization noise
$Q_L$	loaded quality factor
$R$	resistance auto-correlation function
$R_1$	1 <sup>st</sup> resistance of passive loop filter
$R_2$	2 <sup>nd</sup> resistance of passive loop filter
$R_\varphi$	auto-correlation function of random phase $\varphi$
$S$	power spectrum
$S_\varphi$	power spectral density of random phase variation
$S_V$	power spectral density of signal $V(t)$
$t$	time
$t_{on}$	charge-pump turn-on time in locked state
$T$	time temperature
$T_L$	PLL lock-in time (rough estimation)
$T_P$	PLL pull-in time
$T_{ref}$	period of PLL reference signal
$\Delta T_{abs}$	absolute jitter
$\Delta T_{cn}$	cycle-to-average jitter
$\Delta T_{ccn}$	cycle-to-cycle jitter
$u$	unit step function
$v$	voltage
$V$	voltage

$V_c$	VCO control voltage, LF output voltage
$V_p$	output voltage of LF's proportional path
$V_z$	output voltage of LF's integration path
$v_{lf}$	loop filter output voltage noise
$y$	admittance
$z$	impedance
$Z$	impedance, transimpedance
$Z_{lf}$	loop filter transimpedance

---

## Preface

Thanks to the advance of semiconductor and communication technology, the wireless communication market has been booming in the last two decades. It evolved from simple pagers to emerging third-generation (3G) cellular phones. In the meanwhile, broadband communication market has also gained a rapid growth. As the market always demands high-performance and low-cost products, circuit designers are seeking high-integration communication devices in cheap CMOS technology.

The phase-locked loop frequency synthesizer is a critical component in communication devices. It works as a local oscillator for frequency translation and channel selection in wireless transceivers and broadband cable tuners. It also plays an important role as the clock synthesizer for data converters in the analog-and-digital signal interface.

This book covers the design and analysis of PLL synthesizers. It includes both fundamentals and a review of the state-of-the-art techniques. The transient analysis of the third-order charge-pump PLL reveals its locking behavior accurately. The behavioral-level simulation of PLL further clarifies its stability limit. Design examples are given to clearly illustrate the design procedure of PLL synthesizers. A complete derivation of reference spurs in the charge-pump PLL is also presented in this book.

The in-depth investigation of the digital  $\Sigma\Delta$  modulator for fractional-N synthesizers provides insightful design guidelines for this important block. As the prescaler is often the speed bottleneck of high-frequency PLL synthesizers, it is covered in a single chapter in this book. An inherently glitch-free low-power phase-switching prescaler was developed. The timing analysis of the switching control loop gives good understanding for a sound design. As spurs generated from the delay mismatch in the phase-switching



prescaler might be a concern, it is mathematically examined. Another single chapter in this book is devoted to the loop filter, which is an integration bottleneck in narrow-band PLL because its big capacitor takes a large chip area. A simple area-efficient on-chip loop filter solution was proposed. It is based on a capacitance multiplier, which is of very low complexity and power consumption. Detailed analysis and design of this novel loop filter was addressed.

As this book features a complete coverage of PLL synthesizer design and analysis techniques, the authors hope it will be a good manual for both academia researchers and industry designers in the PLL area.

---

## Chapter 1

### INTRODUCTION

#### 1.1 Motivation

In the last decade, the rapid growth of wireless applications has led to an increasing demand of fully integrated, low-cost, low-power, and high-performance transceivers. The applications of wireless communication devices include pagers, cordless phones, cellular phones, global positioning systems (GPS), and wireless local area networks (WLAN), transmitting either voice or data. A standard specifies how devices talk to each other. Numerous standards emerged and are optimized for certain applications. For voice, examples include AMPS, NMT, TACS, D-AMPS, DECT, GSM, DCS, PCS, PDC, TDMA, CDMA, etc. It has evolved from analog to digital, from the 1G (first generation) to the current existing 2.5G, such as GPRS and EDGE. Devices in the 3G wireless standards, which include UMTS (WCDMA), CDMA2000 and TD-SCDMA, are also emerging in some areas of the world. For data, there are 802.11a/b/g WLAN, HiperLAN, Bluetooth, HomeRF, and so on. More recently, a significant interest has grown in the ultra wideband communications [1], [2]. Figure 1-1 briefly illustrates the frequency band of some wireless communication standards.

The recent boom of the mobile telecommunication market has driven worldwide electronic and communication companies to produce small-size, low-power, high-performance and certainly low-cost mobile terminals. The current wireless transceivers involve SiGe bipolar, GaAs and CMOS integrated RF front end and some discrete high-performance components. From a cost of technology point of view, the standard CMOS process is the cheapest one. With a constantly decreasing feature size, it is possible to

design the radio frequency integrated circuits (RFIC) in CMOS technology. A single-chip transceiver with a minimum number of off-chip components is preferred to reduce the cost and size of wireless devices, like cellular phones [3]-[7].

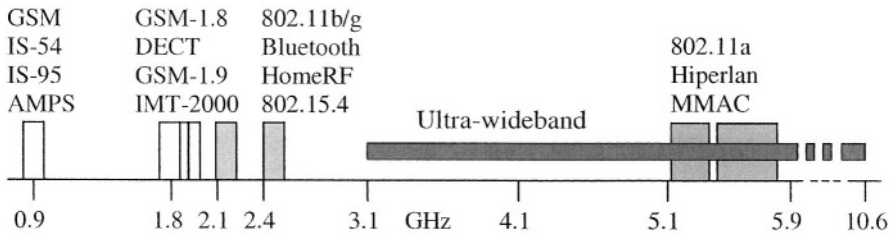


Figure 1-1. Frequency band of wireless communication standards

There are still many difficulties, however, in the process of integration of RF front-end due to the lack of high-quality components on chip. This book focuses on the design of the frequency synthesizer, one of the key building blocks of the RF front-end in CMOS technology. The frequency synthesizer is used as a local oscillator for frequency translation and channel selection in the RF front-end of wireless transceivers. It is a critical component in terms of the performance and cost of a wireless transceiver [8].

## 1.2 Summary of book

This book focuses on both fundamentals and advanced design techniques of PLL-based frequency synthesizers. A 2.4GHz fully integrated  $\Sigma\Delta$  fractional-N frequency synthesizer prototype is implemented in 0.35 $\mu\text{m}$  CMOS technology. Efforts have been put on the prescaler and loop filter, which are the speed and integration bottlenecks, respectively.

A low-power and robust prescaler using an enhanced phase-switching architecture was proposed [9]-[12]. The new architecture is based on generating eight 45°-spaced phases and judiciously arranging the phase-switching sequence to yield an inherently glitch-free phase-switching operation.

In the existing phase-switching architecture [13], the switching is made between four 90°-spaced phases generated by cascading two stages of  $\div 2$  dividers. The prescaler's input frequency is divided by a factor of 4 before switching occurs. Since the frequency of the four signals to be switched by the multiplexer (MUX) is still high, the MUX is usually implemented with current-steering logic and voltage-level amplification is needed. In the proposed enhanced phase-switching architecture, one additional  $\div 2$  divider is used to generate eight 45°-spaced signals. Since the input-signal frequency is

reduced by half, from  $1/4$  to  $1/8$  of the prescaler's input frequency, the MUX can be implemented with standard digital cells to save power consumption and the robustness of phase-switching operation is improved.

Furthermore, the main problem associated with the existing phase-switching architecture is the potential glitches if the switching occurs in the incorrect timing window. Thus, various significant efforts have been made in the literature to yield a glitch-free phase-switching prescaler [13]-[16]. However, all these glitch-removing schemes are not robust and often cost considerable power and area, or even sacrifice the prescaler's maximum operating speed. But in the proposed enhanced phase-switching architecture, an inherently glitch-free phase-switching operation is obtained by means of reversing the switching sequence. Thus, no retiming or synchronization circuit is needed for the switching control and the robustness of the switching operation is guaranteed.

To provide a further insight into the switching operation in the proposed phase-switching architecture, a detailed delay timing analysis of the switching control loop is given. By calculating the delay budget in the loop, we conclude that usually the first  $\div 2$  divider is the only speed constraint of this enhanced phase-switching architecture.

The loop filter is a barrier in fully integrating a narrow-band PLL because of its large integrating capacitor. To make the loop capacitance of a narrow-band PLL as small as possible while keeping the same loop bandwidth, designers increase the loop resistance and reduce the charge-pump current. However, there are practical limitations for both the loop resistance and the charge-pump current. Thermal noise in the large resistor modulates the control voltage and generates phase noise in the VCO, and the charge-pump noise increases while the current decreases.

The dual-path topology has been a popular solution to this problem [17]-[22]. It equivalently scales down the largest integrating and zero-generating capacitance by the scaling factor of the dual charge-pump currents. Besides the increased noise and power due to active devices, the charge-pump of the integration path is still working with a very small current and contributes significant noise. Also, the delay mismatch of the dual charge-pumps may change the loop parameters. Furthermore, at least for the implementations in [18]-[20] and [22], the voltage decay of the low-pass path causes undesirable ripples on the VCO control voltage.

To overcome the constraints of the dual-path topology, a novel loop filter solution is proposed [10]-[12]. A capacitance multiplier [23] is used to reduce the capacitance by a large factor and make it easily integratable within a small chip area.

Besides contributions on the prescaler and loop filter, a comparative study of digital  $\Sigma\Delta$  modulator for fractional-N PLL synthesizers is made [24] to investigate the optimal design of the digital  $\Sigma\Delta$  modulator. A third-order

three-level digital  $\Sigma\Delta$  modulator is employed to reduce the instantaneous phase error at the PFD. The folding of the  $\Sigma\Delta$ -shaped phase noise is minimized by reducing nonlinearities of the PFD and charge pump [10]-[12], [24].

Furthermore, the derivation of the settling time of the third-order PLL, the derivation of spurs due to delay/phase mismatches in the phase-switching prescaler, a complete analysis of the reference spur in the charge-pump PLL, and the behavioral-level verification of the PLL stability limit are all presented in this book.

A prototype chip of the  $\Sigma\Delta$  PLL synthesizer was fabricated in TSMC  $0.35\mu\text{m}$ , 4-metal 2-poly (4M2P) CMOS process through MOSIS. The die size is  $2\text{mm}\times 2\text{mm}$ . It includes a fully integrated  $\Sigma\Delta$  fractional-N frequency synthesizer and some standalone building blocks for testing. The PLL takes an active area of  $0.85\text{mm}^2$ , of which the digital  $\Sigma\Delta$  modulator occupies  $0.5\text{mm}^2$ . With a power supply of 1.5-V for VCO and prescaler, and 2.0-V for other blocks, the whole PLL system consumes  $16\text{mW}$ , of which the VCO consumes  $9\text{mW}$ . With the reference frequency of  $50\text{MHz}$ , the measured phase noise is  $-128\text{dBc/Hz}$  at  $10\text{MHz}$  offset and the reference spur is  $-57\text{dBc}$ .

The proposed prescaler only takes an area of  $0.04\text{mm}^2$ . With a 1.5-V power supply, it works well within the PLL's tuning range of  $2.23\sim 2.45\text{GHz}$  and consumes  $3\text{mW}$ . The proposed loop filter occupies  $0.05\text{mm}^2$  and its power consumption ( $0.2\text{mW}$ ) and noise are negligible compared with the whole PLL.

### 1.3 Book organization

In Chapter 2, the fundamentals of the frequency synthesizer including its features, applications, implementations, and key parameters (jitter and phase noise) are reviewed. Various synthesizer architectures and their pros and cons are discussed.

In Chapter 3, the analysis of the PLL-based frequency synthesizer is covered. It includes the continuous-time linear analysis, discrete-time analysis, stability concerns, operation modes, and fast-locking techniques, etc. An integer-N PLL frequency synthesizer design example is given to illustrate the design procedure.

Chapter 4 concentrates on analysis and design of the  $\Sigma\Delta$  fractional-N PLL frequency synthesizer.  $\Sigma\Delta$  noise mapping methods are reviewed. A comparative study of digital  $\Sigma\Delta$  modulators for fractional-N synthesis is conducted to provide detailed design considerations and guidelines for this block. Other applications of  $\Sigma\Delta$ -PLL are surveyed and a design example of the  $\Sigma\Delta$ -PLL is also included.

Chapter 5 is devoted to the design of the prescaler. The existing design techniques are overviewed. An enhanced, inherently glitch-free phase-switching prescaler is presented. Its architecture and circuit implementation are addressed in great detail. The delay budget of the switching control loop is analyzed to demonstrate its robustness. Furthermore, spurs generated from delay/phase mismatches are derived.

Chapter 6 covers the design of the on-chip loop filter. Current design approaches are addressed. An area- and power-efficient implementation of the on-chip loop filter based on a simple capacitance multiplier is proposed. The detailed design, analysis, and simulation results are provided.

In Chapter 7, the implementation of other building blocks of a  $\Sigma\Delta$  PLL prototype is elaborated. It includes the phase-frequency detector (PFD), the charge-pump (CP), the LC-tuned voltage-controlled oscillator (VCO), the digital  $\Sigma\Delta$  modulator (SDM), and the programmable pulse-swallowing frequency divider. A complete reference spur analysis is also made.

Chapter 8 gives the experimental results of the prototype frequency synthesizer and some standalone building blocks, such as the novel prescaler and loop filter. Measurement results verified the feasibility and robustness of the phase-switching prescaler and the practicality of the loop capacitance multiplier.

Conclusions of this book are drawn in Chapter 9.

Finally, the Matlab simulation of the charge-pump PLL is given in the Appendix. The PLL stability limit is verified through behavioral-level simulations.

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## Chapter 2

# FREQUENCY SYNTHESIZER FOR WIRELESS APPLICATIONS

This chapter describes some fundamentals of frequency synthesizers. It covers the definition, specification, implementation and application of frequency synthesizers. The timing jitter and phase noise, the architecture of frequency synthesizers, and the frequency synthesizer's specification for wireless applications are overviewed.

### 2.1 Definition and characteristics

A frequency synthesizer (FS) is a device that generates one or many frequencies from one or a few frequency sources. Fig. 2-1 illustrates the input and outputs of an FS.

The output of an FS is characterized by its frequency tuning range, frequency resolution, and frequency purity. Ideally, the synthesized signal is a pure sinusoidal waveform. But in reality, its power spectrum features a peak at the desired frequency and tails on both sides. The uncertainty of a synthesizer's output is characterized by its phase noise (or spur level) at a certain frequency offset from the desired carrier frequency in unit of  $dBc/Hz$  (or  $dBc$ ). The unit of  $dBc/Hz$  measures the ratio (in  $dB$ ) of the phase noise power in 1Hz bandwidth at a certain frequency offset to the carrier power. Similarly, the unit of  $dBc$  measures the ratio (in  $dB$ ) of the spur (also known as tone) power at a certain frequency offset to the carrier power. More discussions on the phase noise are covered in the next section. The phase noise requirement of a frequency synthesizer depends on applications. For



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