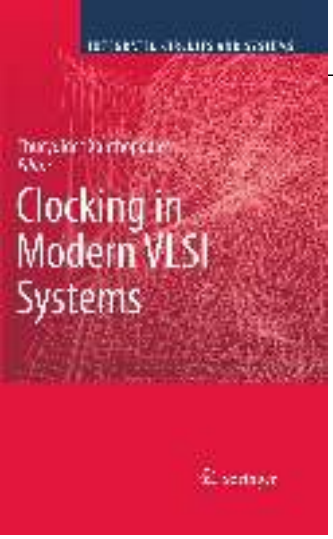
Clocking in
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Thucydides Xanthopoulos
Editor

Clocking in Modern VLSI Systems

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Στη Μαργαρίτα, το Νικόλα και τη Μαρία-Ελένη που μας έπιασε στα μισά
☺

To Margarita, Nicholas and Maria-Helen who joined us half-way
through this book
☺

Preface

... εἰωθότες οἱ ἄνθρωποι οὗ μὲν ἐπιθυμοῦσιν ἐλπίδι ἀπερισκέπτῳ διδόναι, ὃ δὲ μὴ προσίενται λογισμῷ αὐτοκράτορι διωθεῖσθαι.

THUCYDIDIS HISTORIAE IV:108
C. Hude ed., Teubner, Lipsiae MCMXIII

Ὁι ἄνθρωποι, ἄλλωστε, συνειθίζουν νὰ ἐμπιστεύωνται εἰς τὴν ἀπερίσκεπτον ἐλπίδα ἐκεῖνο ποὺ ἐπιθυμοῦν καὶ ν' ἀποκρούουν δι' αὐθαιρέτου συλλογισμοῦ ἐκεῖνο ποὺ ἀποστέργουν.

ΘΟΥΚΥΔΙΔΟΥ ΙΣΤΟΡΙΑΙ Δ:108
Κατά Μετάφρασιν Ἐλευθερίου Βενιζέλου
Δ. Κακλαμάνος Εκδ.
Σμυρνιωτάκης, Αθήνα

It being the fashion of men, what they wish to be true to admit even upon an ungrounded hope, and what they wish not, with a magistral kind of arguing to reject.

Thucydides (the Peloponnesian War Part I), IV:108
Thomas Hobbes Trans., Sir W. Molesworth ed.
In *The English Works of Thomas Hobbes of Malmesbury, Vol. VIII*

I have been introduced to clock design very early in my professional career when I was tapped right out of school to design and implement the clock generation and distribution of the Alpha 21364 microprocessor. Traditionally, Alpha processors exhibited highly innovative clocking systems, always worthy of ISSCC/JSSC publications and for a while Alpha processors were leading the industry in terms of clock performance. I had huge shoes to fill. Obviously, I was overwhelmed, confused and highly confident that I would drag the entire project down. When a few years later

Carl Harris asked me to do a book on clocking for the Springer Integrated Circuits and Systems Series, I readily agreed with the hope that I could save young and aspiring clock designers substantial time and frustration by providing leads and maybe answers to the questions that I had when I was embarking on the Alpha clock design quest. As my choice of opening quotation would suggest, clock design can be a minefield of misconceptions based on little more than a reluctance to apply Kirchhoff's laws, basic constituent relationships, and a little bit of common sense.

In addition to my personal design experience, the choice of material for this book has been heavily informed by my long tenure in the International Solid-State Circuits Conference (ISSCC) program committee. The subjects covered reflect to a large extent the collective interests and foci of both industry and academia with respect to clocking based on ISSCC submissions. The only exception is that there is no coverage of phase locked loop design since there are a number of recent texts available on this subject matter.

It is my hope that this book will help engineers and students interested in clock design obtain the appropriate mental models and design viewpoints, capture design trends that have appeared over the last few years, and provide a comprehensive list of references for further study. I am indebted to my co-authors for providing precise, structured and complete coverage in their respective chapters in addition to maintaining a viewpoint that is very up to date and highly reflective of current trends in the industry. I hope that the reader will not find "ungrounded hopes" and "magistral arguings" in this book.

Carl Harris and Katelyn Stanne of Springer deserve special thanks for helping me throughout the preparation of the manuscript. I wish to acknowledge a number of colleagues at Cavium Networks for their helpful and stimulating discussions and excellent feedback: Scott Meninger, Ethan Crain, David Lin, and Suresh Balasubramanian. I would like to thank my bosses at Cavium Networks Anil Jain and Syed Ali for building a great semiconductor company from the ground up and an excellent working environment that fosters creativity and innovation in addition to maintaining a sharp focus on product development and company value. I would especially like to thank Anil Jain for entrusting me with the Alpha clocking project while being my boss at Compaq Computer which helped me acquire the background and skills necessary to produce this book. Above all, I would like to thank my wife Margarita not only for putting up with my constant working on this book but also for typesetting the entire manuscript in LaTeX and retouching figures as needed. I could not have done this without her.

Boston, Massachusetts *T.X.*
December 2008

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Introduction and Overview

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Clock frequency is a major attribute of any microprocessor design. Early on, during product definition, it constitutes a major business or marketing decision and it is usually the result of a trade-off among customer needs, competitive landscape, and time-to-market. As soon as the frequency target is handed down the food chain to silicon implementation, it will affect all project design aspects from the day that the project is kicked off until it tapes out (and in most cases well beyond this point too). It is not surprising therefore that the job of generating, distributing, and analyzing the clocks in complex chips is considered to be an important and visible assignment. Clock design has traditionally been an area of innovation and has been in the spotlight in technical conferences and journals.

Why is clock frequency such an important microprocessor aspect? For a number of applications it is only loosely correlated with performance with other design aspects such as memory system, parallelism, and hardware acceleration being equally or even more effective. Nevertheless, it is a single number that is widely understood by both technical and nontechnical audiences and in certain situations has strong correlation with single-thread performance.

Clock frequency, although very important, is only one aspect of clock design. Other aspects include power dissipation, efficient clock signal distribution in large and complex chips, coping with variation and uncertainty, managing multiple clock domains in the context of highly integrated system-on-a-chip (SoC) designs, and multicore integration, providing good voltage/frequency scalability to support a wide product roadmap, tuning capabilities for yield enhancement and postsilicon optimization, and sophisticated active power management features.

The purpose of this book is to introduce a designer to important aspects of state-of-the-art clock design by exposing methodology steps and analytical modelling techniques, providing design examples and case studies and enumerating a long list of references for further study.

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