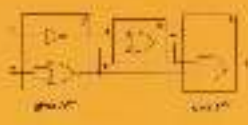


LOGIC SYNTHESIS
AND
VERIFICATION
ALGORITHMS



Gary D. Hachtel
Fabio Somenzi

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by

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To:

Linda, Jordan, and Kira,

and

Chiara and Laura.

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